REMARKS

Claims 5-12 have been canceled without prejudice or disclaimer. Claims 1-4 have been amended. Accordingly, claims 1-4 are currently pending in the application.

PRIORITY

Enclosed is a certified copy of foreign priority document JP No. 2000-375686, filed December 11, 2000. Applicants request the Examiner to acknowledge the safe receipt of the certified priority document.

TITLE OF THE INVENTION

The title of the invention has been amended into a more descriptive form as required by the Examiner.

35 U.S.C. §112

Claim 3 has been amended to overcome the outstanding rejection under 35 U.S.C. §112, second paragraph. Claim 6 has been canceled without prejudice or disclaimer.

35 U.S.C. §102

Claims 1-6 and 10-12 stand rejected under 35 U.S.C. §102 as being anticipated by Takeuchi et al. This rejection is traversed as follows.

The present invention is directed to a non-volatile semiconductor memory device having a memory cell array. Each of the memory cells of the memory cell array has plural numbers of charge storage grains that are independent from each other and insulated. Therefore, upon the occurrence of a leak path, the charge of one grain near the leak path of the charge storage area of the memory may be loosened. As a result, only a part of the stored information in the plurality of grains forming the memory cell is destroyed and it is possible to hold information in a stable manner (See Specification page 16, lines 2-11).

Takeuchi et al disclose a semiconductor device having a plurality of memory cells, each having one charge storage region. Therefore, Takeuchi et al do not disclose that each memory cell has plural charge storage regions as in the present invention. As shown in Figure 2A of Takeuchi et al, each charge storage region (14_1, 14_2, ... 14_8) corresponds to

each of memory cells (M_1, M_2 ... M_8). Therefore, each memory cell has only one charge storage region.

As a result, unlike in the present invention, when a leak path occurs in a memory cell of Takeuchi et al, the information stored in that memory cell is lost, as opposed to just the charge of one grain near the leak path as in the present invention. As such, it is submitted that the pending claims patentably define the present invention over the cited art.

35 U.S.C. §103

Claims 7-9 stand rejected under 35 U.S.C. §103 as being unpatentable over Takeuchi et al. This rejection has been rendered moot in view of the cancellation of those claims without prejudice or disclaimer.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is

now in condition for allowance. Accordingly, reconsideration and reexamination are respectfully requested.

Respectfully submitted,

Shrinath Malur
Registration No. 34,663
Attorney for Applicants

MATTINGLY, STANGER & MALUR
1800 Diagonal Rd., Suite 370
Alexandria, Virginia 22314
(703) 684-1120
Date: February 25, 2003